Amplifier Transistors

NPN Silicon

Features

• These are Pb-Free Devices*

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Collector - Emitter Voltage	V _{CEO}	40	Vdc
Collector - Base Voltage	V _{CBO}	75	Vdc
Emitter – Base Voltage	V _{EBO}	6.0	Vdc
Collector Current – Continuous	I _C	600	mAdc
Total Device Dissipation @ T _A = 25°C Derate above 25°C	P _D	625 5.0	mW mW/°C
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

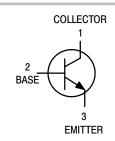
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

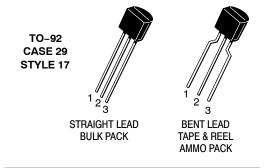
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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MARKING DIAGRAM



A = Assembly Location

Y = Year WW = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
P2N2222AG	TO-92 (Pb-Free)	5000 Units/Bulk
P2N2222ARL1G	TO-92 (Pb-Free)	2000/Tape & Ammo

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS	-			
Collector – Emitter Breakdown Voltage $(I_C = 10 \text{ mAdc}, I_B = 0)$	V _(BR) CEO	40	-	Vdc
Collector – Base Breakdown Voltage $(I_C = 10 \mu Adc, I_E = 0)$	V _{(BR)CBO}	75	_	Vdc
Emitter – Base Breakdown Voltage $(I_E = 10 \mu Adc, I_C = 0)$	V _{(BR)EBO}	6.0	-	Vdc
Collector Cutoff Current (V _{CE} = 60 Vdc, V _{EB(off)} = 3.0 Vdc)	I _{CEX}	_	10	nAdc
Collector Cutoff Current (V _{CB} = 60 Vdc, I _E = 0) (V _{CB} = 60 Vdc, I _E = 0, T _A = 150°C)	I _{CBO}	- -	0.01 10	μAdc
Emitter Cutoff Current (V _{EB} = 3.0 Vdc, I _C = 0)	I _{EBO}	_	10	nAdc
Collector Cutoff Current (V _{CE} = 10 V)	I _{CEO}	_	10	nAdc
Base Cutoff Current (V _{CE} = 60 Vdc, V _{EB(off)} = 3.0 Vdc)	I _{BEX}	-	20	nAdc
ON CHARACTERISTICS	•	•	1	•
$\begin{array}{l} \text{DC Current Gain} \\ (I_C = 0.1 \text{ mAdc, } V_{CE} = 10 \text{ Vdc)} \\ (I_C = 1.0 \text{ mAdc, } V_{CE} = 10 \text{ Vdc)} \\ (I_C = 10 \text{ mAdc, } V_{CE} = 10 \text{ Vdc)} \\ (I_C = 10 \text{ mAdc, } V_{CE} = 10 \text{ Vdc, } T_A = -55^{\circ}\text{C)} \\ (I_C = 150 \text{ mAdc, } V_{CE} = 10 \text{ Vdc, } (\text{Note 1}) \\ (I_C = 150 \text{ mAdc, } V_{CE} = 1.0 \text{ Vdc)} \text{ (Note 1)} \\ (I_C = 500 \text{ mAdc, } V_{CE} = 10 \text{ Vdc)} \text{ (Note 1)} \\ \end{array}$	h _{FE}	35 50 75 35 100 50 40	- - - 300 -	-
Collector – Emitter Saturation Voltage (Note 1) $ \begin{pmatrix} I_{C} = 150 \text{ mAdc, } I_{B} = 15 \text{ mAdc} \\ I_{C} = 500 \text{ mAdc, } I_{B} = 50 \text{ mAdc} \end{pmatrix} $	V _{CE(sat)}	_ _	0.3 1.0	Vdc
Base – Emitter Saturation Voltage (Note 1) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	V _{BE(sat)}	0.6 -	1.2 2.0	Vdc
SMALL-SIGNAL CHARACTERISTICS	•	•		•
Current – Gain – Bandwidth Product (Note 2) (I _C = 20 mAdc, V _{CE} = 20 Vdc, f = 100 MHz)C	f _T	300	-	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{obo}	_	8.0	pF
Input Capacitance (V _{EB} = 0.5 Vdc, I _C = 0, f = 1.0 MHz)	C _{ibo}	-	25	pF
Input Impedance $ (I_C = 1.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}) $ $ (I_C = 10 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}) $	h _{ie}	2.0 0.25	8.0 1.25	kΩ
Voltage Feedback Ratio ($I_C = 1.0 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$) ($I_C = 10 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h _{re}	- -	8.0 4.0	X 10 ⁻⁴
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h _{fe}	50 75	300 375	-
Output Admittance ($I_C = 1.0 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$) ($I_C = 10 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h _{oe}	5.0 25	35 200	μMhos
Collector Base Time Constant (I _E = 20 mAdc, V _{CB} = 20 Vdc, f = 31.8 MHz)	rb′C _c	-	150	ps
Noise Figure (I _C = 100 μ Adc, V _{CE} = 10 Vdc, R _S = 1.0 k Ω , f = 1.0 kHz)	N _F	_	4.0	dB

^{1.} Pulse Test: Pulse Width $\leq 300~\mu s$, Duty Cycle $\leq 2.0\%$. 2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

	Characteristic	Symbol	Min	Max	Unit
SWITCHING CHARAC	CTERISTICS				
Delay Time	$(V_{CC} = 30 \text{ Vdc}, V_{BE(off)} = -2.0 \text{ Vdc},$	t _d	-	10	ns
Rise Time	$I_C = 150 \text{ mAdc}, I_{B1} = 15 \text{ mAdc}) \text{ (Figure 1)}$	t _r	-	25	ns
Storage Time	(V _{CC} = 30 Vdc, I _C = 150 mAdc,	t _s	-	225	ns
Fall Time	$I_{B1} = I_{B2} = 15 \text{ mAdc}$ (Figure 2)	t _f	_	60	ns

SWITCHING TIME EQUIVALENT TEST CIRCUITS

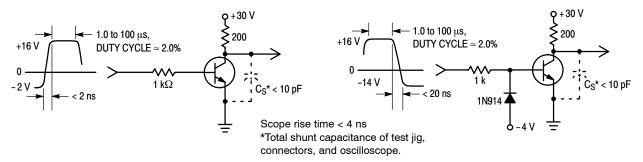


Figure 1. Turn-On Time

Figure 2. Turn-Off Time

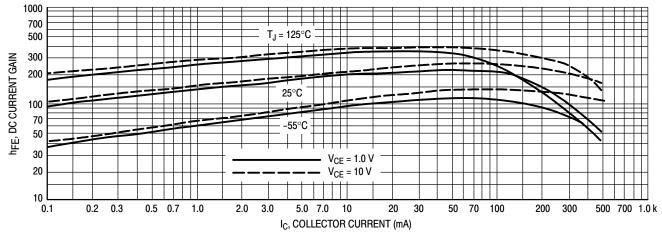


Figure 3. DC Current Gain

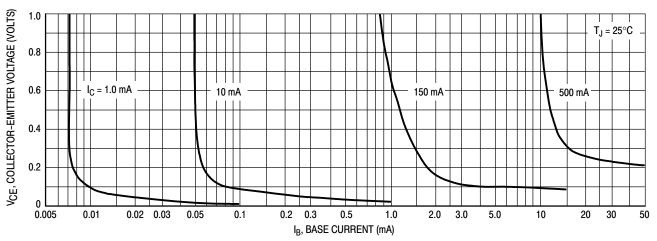


Figure 4. Collector Saturation Region

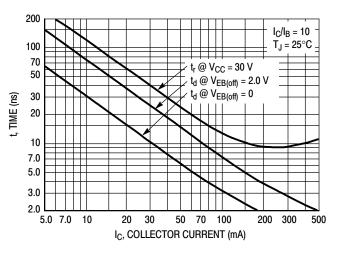


Figure 5. Turn-On Time

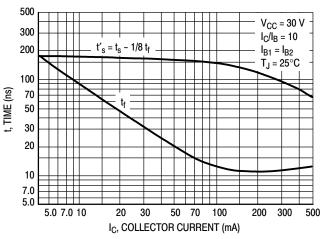


Figure 6. Turn – Off Time

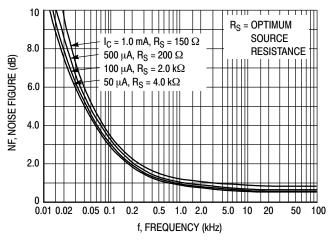


Figure 7. Frequency Effects

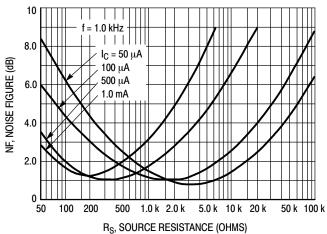
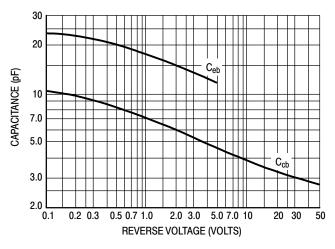


Figure 8. Source Resistance Effects

+0.5



T_J = 25°C

T_J = 25°C

T_J = 25°C

1.0

2.0

3.0

5.0

1.0

2.0

3.0

5.0

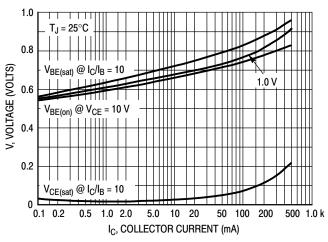
7.0

100

1_C, COLLECTOR CURRENT (mA)

Figure 9. Capacitances

Figure 10. Current-Gain Bandwidth Product



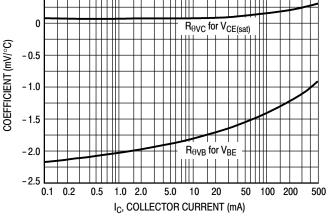
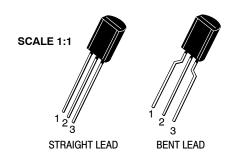


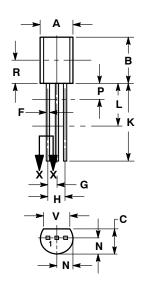
Figure 11. "On" Voltages

Figure 12. Temperature Coefficients



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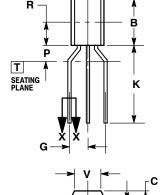
DATE 08 MAY 2012



STRAIGHT LEAD



BENT LEAD





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- 714.5M, 1994.
 CONTROLLING DIMENSION: INCHES.
 CONTOUR OF PACKAGE BEYOND DIMENSION R IS
 UNCONTROLLED.
- UNIONI HOLLEU, DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L DIMENSIONS D AND J APPLY BETWEEN DI-MENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INC	HES	MILLIM	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.175	0.205	4.44	5.21
В	0.290	0.310	7.37	7.87
С	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
Н	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500		12.70	
L	0.250		6.35	
N	0.080	0.105	2.04	2.66
Р		0.100		2.54
R	0.135		3.43	
٧	0.135		3.43	

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME
- CONTROLLING DIMENSION: INCHES.
 CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
- DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

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DIM	MIN	MAX	MIN	MAX
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D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500		12.70	
N	0.080	0.105	2.04	2.66
P		0.100		2.54
R	0.135		3.43	
٧	0.135		3.43	

STYLES ON PAGE 2

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ISSUE A

DATE 08 MAY 2012

STYLE 1: PIN 1. 2. 3.	EMITTER BASE COLLECTOR	STYLE 2: PIN 1. 2. 3.	BASE EMITTER COLLECTOR	STYLE 3: PIN 1. 2. 3.	ANODE ANODE CATHODE	STYLE 4: PIN 1. 2. 3.	CATHODE CATHODE ANODE	STYLE 5: PIN 1. 2. 3.	DRAIN SOURCE GATE
	GATE SOURCE & SUBSTRATE DRAIN	STYLE 7: PIN 1. 2. 3.	SOURCE DRAIN GATE	STYLE 8: PIN 1. 2. 3.	DRAIN GATE SOURCE & SUBSTRATE	STYLE 9: PIN 1. 2. 3.	BASE 1 EMITTER BASE 2	STYLE 10: PIN 1. 2. 3.	CATHODE GATE ANODE
2.	ANODE CATHODE & ANODE CATHODE	STYLE 12: PIN 1. 2. 3.	MAIN TERMINAL 1 GATE MAIN TERMINAL 2	STYLE 13: PIN 1. 2. 3.	ANODE 1 GATE CATHODE 2	STYLE 14: PIN 1. 2. 3.	EMITTER COLLECTOR BASE	STYLE 15: PIN 1. 2. 3.	ANODE 1 CATHODE ANODE 2
PIN 1. 2.	ANODE	PIN 1.	COLLECTOR BASE EMITTER	STYLE 18: PIN 1. 2. 3.	ANODE	STYLE 19: PIN 1. 2. 3.	GATE ANODE CATHODE	2.	NOT CONNECTED CATHODE ANODE
PINI 1	COLLECTOR EMITTER BASE	PIN 1.	SOURCE	PIN 1.	GATE	PIN 1. 2.	EMITTER	PIN 1. 2.	MT 1
	V _{CC} GROUND 2 OUTPUT	STYLE 27: PIN 1. 2. 3.	MT SUBSTRATE MT	2.	CATHODE ANODE GATE	2.	NOT CONNECTED ANODE CATHODE	2.	DRAIN GATE SOURCE
PIN 1. 2.	GATE DRAIN SOURCE	PIN 1.	BASE	PIN 1. 2.	RETURN INPUT OUTPUT	PIN 1. 2.	INPUT GROUND LOGIC		

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DESCRIPTION:	TO-92 (TO-226) 1 WATT		PAGE 2 OF 2	

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